UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/920,853	08/03/2001	Jae-Hyuk Lee	P-242	6667

34610 7590 08/09/2005

FLESHNER & KIM, LLP
P.O. BOX 221200
CHANTILLY, VA 20153

EXAMINER	
KUMAR, PANKAJ	
ART UNIT	**PAPER NUMBER**
2631	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/920,853	LEE, JAE-HYUK	
	Examiner	Art Unit	
	Pankaj Kumar	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,8,9,16-20 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23-26,28-35 and 37* is/are allowed.

6)☒ Claim(s) *1,8,9,16-20,22 and 27* is/are rejected.

7)☒ Claim(s) *2-7 and 11-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Response to Amendment

Claim Objections

2. Claim 27 is objected to because of the following informalities: the first recitation of current digital input signal should be preceded by 'a' instead of "the". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 8, 9, 16-20, 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Ha WO 00/08870. Here is how the reference teaches the claims:

5. As per claim 1: A predistortion digital linearizer, comprising a predistorter coupled to receive an input signal and a control signal to generate a predistorted signal (Ha fig. 2: 170 with 102, 104); an up-converter coupled to receive the predistorted signal and convert it into a radio

frequency signal (Ha fig. 2: 114), a high power amplifier (HPA) to receive and amplify the radio frequency signal outputted from the up-converter (Ha fig. 2: 122); a feedback unit coupled to receive an output of the HPA and down-convert the received signal into a baseband signal (Ha fig. 2: bottom output of 124 to 142, 144), an adaptation processing unit coupled to receive the baseband signal (Ha fig. 2: outputs of 144) and a delayed digital input signal (Ha fig. 2: 158) to generate the control signal (Ha fig. 2: bottom inputs into 170), the adaptation processing unit including: a delay unit to delay the input signal for a prescribed period of time (Ha fig. 2: inherent for delay 158 to be for a prescribed period of time); and a digital signal processor (Ha fig. 2: elements 164, 166, 160, 162, 154, 156, etc. comprise DSP) coupled to receive the delayed input signal (Ha fig. 2: 158) and the baseband signal from the feedback unit (Ha fig. 2: bottom output of 124 to 142, 144) to generate the control signal (Ha fig. 2: bottom inputs into 170).

6. As per claim 8: The device of claim 1, wherein the input signal is a digital input signal and the predistorted signal is a predistorted digital signal, and wherein the up-converter comprises first and second digital-to-analog converters to convert the predistorted digital signal to an analog signal (Ha fig. 2: 106, 108); and a modulator to modulate the analog signal outputted from the digital-to-analog converters (Ha fig. 2: 114).

7. As per claim 9. The device of claim 1, wherein the feedback unit comprises a demodulator to demodulate the output of the HPA (Ha fig. 2: 144); and first and second analog-to-digital converters to convert the demodulated analog signal outputted from the demodulator to a digital signal (Ha fig. 2: 150, 152).

8. As per claim 16: The device of claim 1, wherein the predistorted digital signal has a distortion characteristic that is opposite of a distortion characteristic of the HPA such that an output of the HPA is substantially non-distorted (Ha: this is the purpose of predistortion).

9. As per claim 17: The device of claim 1, wherein each of the input signal, the predistorted signal, and the baseband signal is a digital signal (Ha fig. 2: these are all before D/A and after A/D).

10. As per claim 18, a predistortion digital linearizer, comprising a digital predistorter to distort a digital input signal according to a control signal (Ha fig. 2: 170 with 102, 104), the digital input signal comprises first and second digital input signals, the first digital input signal having a different phase than the second digital input signal (Ha fig. 2: i-phase (ui) and q-phase (uq) as are inputs into 160 and 162 which eventually connects to 170), and wherein the digital predistorter separately distorts the first and second digital input signals to provide first and second output signals (Ha fig. 2: separate inputs and outputs into 170 with 102, 104); a digital-to-analog converter comprising first and second digital-to-analog converters to convert the respective output signals of the digital predistorter to analog signals (Ha fig. 2: 106, 108); a modulator coupled to modulate an output signal of the digital-to-analog converter to a frequency of a carrier (Ha fig. 2: 114); a high power amplifier (HPA) coupled to power-amplifier an output signal of the modulator (Ha fig. 2: 122); a demodulator coupled to receive an output signal of the HPA and demodulate it to a baseband signal (Ha fig. 2: 144); an analog-to-digital converter coupled to convert the analog baseband signal outputted from the demodulator to a digital signal, the analog-to-digital converter comprises first and second analog-to-digital converters to convert first and second analog baseband signals to first and second digital feedback signals (Ha fig. 2:

150, 152); and a digital signal processor (Ha fig. 2: elements 164, 166, 160, 162, 154, 156, etc. comprise DSP) coupled to compare an output signal of the analog-to-digital converter (Ha fig. 2: 150, 152) to the digital input signal (Ha fig. 2: left inputs into 154, 156) and generate the control signal to control a distortion degree of the digital predistorter (Ha fig. 2: bottom inputs into 170), wherein the digital signal processor uses each of the first and second digital feedback signals to generate the control signal (Ha fig. 2: outputs of 150, 152 being used in the DSP).

11. As per claim 19, it is discussed above with respect to claim 16

12. As per claim 20, the device of claim l 8: further comprising a coupler to receive and split off a portion of the output signal of the HPA and provide the split off portion to the demodulator (Ha fig. 2: 124)

13. As per claim 22. The device of claim 18, wherein the digital signal processor generates first and second control signals to control each of the first and second digital input signals separately (Ha fig. 2: control signals through 170 which eventually control the left inputs into 102, 104).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oishi 6,567,478 in view of Carsello 5,566,213. Here is how the references teach the claim:

16. As per claim 27: A method for controlling a gain of a predistortion digital linearizers comprising: determining an output level of a high power amplifier (Oishi fig. 15: 34; col. 6 line 44) using a feedback digital output signal (Oishi fig. 15: 35 to 55); computing a gain control signal for gain control (Oishi fig. 15, 19: 38) by using the determined output level (Oishi fig. 15, 19: output from 35), a desired output level (Oishi fig. 15: output from 71; fig. 19: X1..X4), and a level of a digital input signal delayed for a prescribed period of time (Oishi fig. 21: input into 81g, 81c, etc. has been delayed by the prescribed time period of the time it takes for the signal to go through the elements 51, 52, 72, 53); multiplying the current digital input signal (object: change the to a) by the gain control signal to control the level of the digital input signal; and maintaining a sign bit of a multiplication resulting value, taking remaining lower bits as a predetermined number of bits, and adjusting digits of the digital input signal before and after multiplication (not in Oishi but would be obvious as explained below).

17. Oishi does not teach multiplying the current digital input signal by the gain control signal to control the level of the digital input signal; and maintaining a sign bit of a multiplication resulting value, taking remaining lower bits as a predetermined number of bits, and adjusting digits of the digital input signal before and after multiplication. Carsello teaches multiplying the current digital input signal by the gain control signal to control the level of the digital input signal (Carsello 5566213 fig. 2: 68); and maintaining a sign bit of a multiplication resulting value (Carsello fig. 2: after multiplication in 68, sign determined in 110), taking remaining lower bits as a predetermined number of bits (Carsello fig. 3b: various sections of bits), and adjusting digits of the digital input signal before and after multiplication (Carsello fig. 2: bits of the digital signal is adjusted before and after multiplication in 68). Thus, it would have been obvious, to one of

ordinary skill in the art, at time the invention was made, to arrive at the multiplying the current digital input signal by the gain control signal to control the level of the digital input signal; and maintaining a sign bit of a multiplication resulting value, taking remaining lower bits as a predetermined number of bits, and adjusting digits of the digital input signal before and after multiplication as recited by the instant claims, because the combined teaching of Oishi with Carsello suggest multiplying the current digital input signal by the gain control signal to control the level of the digital input signal; and maintaining a sign bit of a multiplication resulting value, taking remaining lower bits as a predetermined number of bits, and adjusting digits of the digital input signal before and after multiplication as recited by the instant claims. Furthermore, one of ordinary skill in the art, would have been motivated to combine the teachings of Oishi with Carsello because Oishi suggests various calculations including addition, subtraction, and multiplication of digital bits (such as Oishi fig. 2, 3, 4, 5, 11, etc.) (something broad) in general and Carsello suggests the beneficial use of improving symbol decoding (Carsello: title) and not have false lock points (Carsello col. 1 lines 54-67) and reduce jitter (Carsello col. 1 lines 45-53) by doing multiplication as claimed (in the analogous art of feeding back output with gain control.

Allowable Subject Matter

18. Claims 2-7, 11-15 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. Claim 23 is allowable. The following is a statement of reasons for the indication of allowable subject matter for claim 23: The art of record does not suggest the respective claim

combinations together and nor would the respective claim combinations be obvious with: a gain control circuit to receive and control a level of a digital input signal according to a gain control signal; predistorter coupled to predistort the gain controlled digital input signal in accordance with a control signal.

20. Claims 24-26 are allowable since they depend on claim 23.

21. Claim 28 is allowed based on amendments. Accordingly, claims 29-35 and 37 are also allowable.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (571) 272-3011. The examiner can normally be reached on Mon, Tues, Thurs and Fri after 8AM to after 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pankaj Kumar
Patent Examiner
Art Unit 2631

PK

M. Gh

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER